REMARKS

The application contains claims 1-7, 9-20, 22-30, and 38-43. Claims 4-7 are allowed, and claims 17-19 are identified as allowable. In view of the foregoing amendment and following remarks, Applicants respectfully request allowance of the application.

Applicants thank Dr. Tsai for the courtesy of the September 10, 2004 interview with Applicants' representative. At that meeting, Applicants' representative presented arguments in rebuttal of the rejections made in the June 3, 2004 Office Action. These arguments are repeated in this response.

PREVIOUSLY ALLOWED CLAIMS

Claims 9-16 and 23-27 have been previously allowed, but now stand rejected for various reasons. MPEP § 706.04 requires that a claim noted as allowable shall thereafter be rejected only with great care. MPEP § 706.04 also states that, because it is unusual to reject a previously allowed claim, the examiner should point out in his or her office action that the claim now being rejected was previously allowed by using Form paragraph 7.50. Typically, previously allowed claims are rejected only in view of a newly discovered prior art reference. Here, however, the indicated allowability of these claims could not have been withdrawn in view of a newly discovered prior art reference because other claims were rejected based on Agarwal (U.S. Patent No. 5,966,541) in previous Office Actions. The June 3 Office Action also does not point out why the allowability of these claims has been withdrawn. Applicants respectfully request the Examiner to reconsider these rejections and/or to point out in his Office Action why the allowability of these claims has been withdrawn.

CLAIM OBJECTIONS

The foregoing amendments are provided to overcome the claim objections made in the Office Action. Accordingly, Applicants respectfully request withdrawal of the claim objections.

THE § 101 REJECTIONS SHOULD BE WITHDRAWN.

Applicants respectfully request withdrawal of the section 101 rejections to claims 1-3, 9-15, 20, 22 and 28-30. These claims clearly recite subject matter that is concrete, tangible and useful. Therefore, the claims are statutory.

Independent Claims 1 and 20 are Statutory.

Consider claims 1 and 20, which recite:

> apparatus, comprising a *memory entry* storing a trace having a multiple-entry, single exit architecture [claim 1]; and
>
> apparatus, comprising a *memory entry* storing a sequence of program instructions as a trace [claim 20].

These claims recite statutory and functionally descriptive material. The term "memory entry" clearly refers to apparatus, which is statutory per se. See, In re Warmerdam, 33 F.3d 1354, 1360-61 (Fed. Cir. 1994). This terminology is a clear reference to computer-readable apparatus (i.e., memory structures, such as caches, queues, ROMs, and RAMs) that conventionally organized into a plurality of memory entries. Additionally, however, as indicated during the interview, the reference to the multiple-entry, single exit architecture of the traces stored therein is a clear reference to functional descriptive material as explained in the MPEP's guidelines for examination of computer-related inventions. See MPEP § 2106 (IV)(B)(1)(a) (2100-13) ("a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships, ..., and is thus statutory.").

Applicants respectfully dispute the Office Action's assertion that memory entry is an abstract reference to memory size, in a manner similar to terms such as "inch" or "foot." This interpretation is inappropriate in light of the specification and ordinary meanings of the term. Memories store data. Claims 1 and 20 both indicate that a memory entry *stores* a trace having the characteristics set forth in their respective claims. The claims have a meaning that is perfectly clear. Applicants respectfully submit the Office Action's construction of the claim language is incorrect.

Independent Claim 9 is Statutory.

The Office Action also contends that claim 9 is directed to non-statutory subject matter because "the method steps can be mental steps." This is not the test for statutory subject matter. The test merely requires that the claims recite subject matter that is concrete, tangible and useful. Claim 9 clearly meets these requirements.

The claimed invention as recited in claim 9 provides a method that contributes to reduced redundancy when stored in a memory. Thus, it is clear that the claimed invention

defines a method that is useful in the internal operation of a processor, which is also within the "useful art." The claimed method recited in claim 9 is, therefore, a statutory method (or process) within the meaning of 35 U.S.C. § 101.

Independent Claim 28 is Statutory.

Claim 28 recites:

> A trace, comprising a sequence of program instruction assembled in order according to program flow, the sequence having a multiple-entry, single exit architecture [claim 28]

A trace also is a statutory element. Ordinary engineers in the field recognize it as an artifact that imposes substantive performance improvements to processing devices. See, for example, The New IEEE Standard Dictionary of Electrical and Electronics Terms 1388 (5th ed. 1993). Claim 28 refers to a specific trace architecture, which is believed to provide substantial performance improvements over other traces that were known previously. For example, use of the new trace architecture will reduce redundancy when they are stored in a trace cache, which improves overall performance of a processing device. See, Specification, p. 3. These are *functional* performance improvements provided by the invention. This is not non-functional descriptive material, such as music or poetry. This invention makes processors and other devices work better.

Moreover, the statement of utility required under 35 U.S.C. § 101 is not limited to an "actual use" statement, but an indication of intended use also suffices to meet the statutory subject matter requirement. See In re Bremner, 37 CCPA 1032, In re Kirchner, 305 F.2d 897, 899 (CCPA 1968). Accordingly, claim 28 satisfies the statement of utility required under 35 U.S.C. § 101.

Applicants respectfully submit that the § 101 rejections to claims 1, 9, 20, and 28 are clearly wrong and request that it be withdrawn. For the same reasons, the § 101 rejections to claims 2-3, 10-15, 22, and 29-30, which depend from independent claims 1, 9, 20, and 28 should also be withdrawn.

THE § 112, SECOND PARAGRAPH REJECTIONS SHOULD BE WITHDRAWN.

Claims 1-3, 20, 22, and 28-30 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicants regard as the invention. In particular, the Office Action contends that the terms "a memory entry," "a trace," and "a sequence of program instructions" are not hardware elements, and thus, the real claimed invention is unclear. Section 112, second paragraph, does not limit claims to a list of hardware elements; it merely requires the claims to be clear. These terms are clear. As discussed earlier, memory entries are some of the most basic elements in computer architectures. The term "Trace" is a well-understood term; it appears in technical dictionaries. "Program instructions" is another simple, straightforward concept in the computer arts. Surely, the Examiner cannot seriously dispute that he does not understand what these terms mean.

Applicants note that, while these claims are short, they are directed to precisely the subject matter that the inventors regard as their invention. In this regard, the MPEP indicates this claiming structure is preferred:

> In fact, it is preferable for claims to be drafted in a form that emphasizes what the applicant has invented (i.e., what is new rather than old).

MPEP § 2106, p. 2100-19. This is exactly what is occurring here. The claims are clear, they use straightforward language that is well understood by persons of ordinary skill, and they are directed squarely at the invention. These claims satisfy the requirements of the § 112, second paragraph. Accordingly, Applicants respectfully request withdrawal of the outstanding § 112, second paragraph, rejections to claims 1-3, 20, 22, and 28-30.

THE §102 REJECTIONS SHOULD BE WITHDRAWN.

Claims 1-3, 16, 20, 22, and 28-30 stand rejected under 35 U.S.C. § 102 as anticipated by Agarwal (U.S. Patent No. 5,966,541). Applicants respectfully request withdrawal of these rejections because Agarwal does not disclose all elements of claims 1-3, 16, 20, 22, and 28-30.

Claim 1 recites:

> Apparatus, comprising a memory entry storing a trace having a multiple-entry, single exit architecture.

Agarwal does not disclose this subject matter. The Office Action contends that a program flow illustrated in FIG. 8 of Agarwal discloses the claimed features of claim 1. In particular, the Office Action contends that blocks 101, 102, and 103 constitute a memory entry to store a trace having a multiple-entry, single exit architecture. Applicants respectfully disagree. FIG. 8 is a

program flow diagram illustrating a generic execution sequence of instructions I0-I9, where instructions I0-I9 are organized into "blocks." A block is a sequence of instructions without a branch or jump instruction. Thus, Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Agarwal, col. 11, lines 17-20. More importantly, Agarwal does not disclose whether and/or how these blocks are stored in a memory entry, but simply that "some memory is associated with each program block". See Agarwal, col. 11, lines 36-38. Thus, Agarwal fails to disclose a memory entry storing a trace having a multiple-entry, single exit architecture. Accordingly, claim 1 defines over the art. Claims 2 and 3, which depend from independent claim 1, also define over the art.

Claim 16 recite:

> A front-end stage storing blocks of instructions in a multiple-entry, single exit architecture when considered according to program flow.

Agarwal does not disclose this subject matter. The Office Action contends that Agarwal discloses a memory (703 in FIG. 11) that stores instructions in a multiple-entry, single exit architecture. Applicants respectfully disagree. Again, Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Agarwal, col. 11, lines 17-20. More importantly, Agarwal fails to disclose whether and/or how these blocks are stored in a front-end stage having a multiple-entry, single exit architecture. Accordingly, Agarwal fails to anticipate the claimed invention as recited in claim 16. Thus, Applicants respectfully request withdrawal of the § 102(e) rejection of claim 16.

Claim 20 recites:

> A computer-readable apparatus, comprising a memory entry storing a sequence of program instructions as a trace, the instructions defining a program flow that progresses from any instruction therein to a last instruction in the memory entry and in which the trace has multiple separate prefixes.

Agarwal does not disclose this subject matter. The Office Action contends that the program flow shown in FIG. 8 of Agarwal progresses from any instruction to a last instruction in a trace. Applicants respectfully disagree. As explained above, Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. Moreover, the program flow is defined by putting together multiple instruction blocks in a sequential order. Thus, Agarwal's program flow cannot progress from any instruction to a last

instruction in the memory entry. Rather, Agarwal's program flow must start with instruction I0 of the first block and end with instruction I9 of the last block. Accordingly, claim 20 defines over the prior art. Claim 22, which depends from independent claim 20, also defines over the prior art.

Claim 28 recites:

> A trace, comprising a sequence of program instruction assembled in order according to program flow, the sequence having a multiple-entry, single exit architecture.

Agarwal does not disclose this subject matter. The Office Action contends that a program flow illustrated in FIG. 8 of Agarwal discloses the claimed features of claim 1. In particular, the Office Action contends that blocks 101, 102, and 103 have a multiple-entry, single exit architecture. Applicants respectfully disagree. Agarwal does not disclose a trace, or any equivalent structure thereof. Additionally, Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Agarwal, col. 11, lines 17-20. More importantly, Agarwal does not disclose whether and/or how these blocks are stored in a trace. Thus, Agarwal fails to disclose a trace comprising an program instruction sequence having a multiple-entry, single exit architecture. Accordingly, claim 28 defines over the art. Claims 29 and 30, which depend from independent claim 28, also define over the art.

THE §103 REJECTIONS SHOULD BE WITHDRAWN.

Claims 23-27 stand rejected under 35 U.S.C. § 103 as being obvious over Agarwal. Applicants respectfully request withdrawal of these rejections because Agarwal does not render claims 23-27 obvious.

Claim 23 recites:

> A memory comprising storage for a plurality of traces and means for indexing the traces by an address of a last instruction therein according to program flow.

The Office Action contends that Agarwal's entry is "inherently" indexed by an address of a last instruction. The Office Action also contends that "it would have been obvious to one having ordinary skill in the art at the time of invention to modify Agarwal's machine to comprise a memory comprising means for indexing the traces by an address of a last instruction." The

Office Action, however, fails to provide any suggestion or motivation to modify Agarwal to arrive at the claimed invention as recited in claim 23. Moreover, contrary to the Office Action's contention that such indexing scheme is a mere alternative arrangement, no memory, at least to the undersigned's knowledge, indexes its traces "by an address of a last instruction therein according to program flow." Thus, the § 103 rejection is improper. Accordingly, Applicants respectfully request withdrawal of the § 103 rejection to claim 23. For the same reasons, the § 103 rejections to claims 24-27 should also be withdrawn.

NEW CLAIMS

New claims 38-43 are presented for examination. Of these claims, claims 38-40 are added as per the Examiner's recommendation. In view of the foregoing, all newly added claims are believed to recite statutory subject matter that define over the cited art.

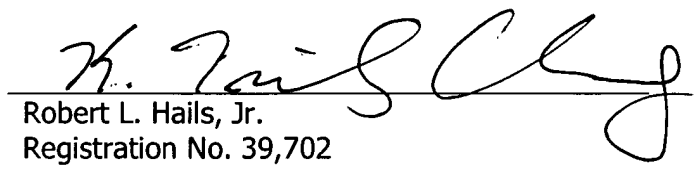
CONCLUSION

In view of the above amendments and remarks, Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

The Office is authorized to charge any fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

Date: 10/4/04



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